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(54) Drive circuit for active matrix type liquid crystal display device.

(57) In the drive circuit of an active matrix type liquid crystal display device of this invention, the digital video signal having m-bit gray-scale is inputted to the serial parallel converter (1) and converted to the parallel video data corresponding to one line, and the (m-1) bit gray-scale data excluding the least significant bit is outputted to adders (121, 122, ..., 12n). During the first period, this (m-1) bit gray-scale data is supplied to decoders (21, 22, ..., 2n), from the adders (121, 122, ..., 12n), and during the second period, the least significant bit is added to this (m-1) bit gray-scale data at adders in accordance with the lest significant bit of the video data and supplied to decoders (21, 22, ..., 2n), respectively. In the voltage selector (31, 32, ..., 3n), with the output from decoders (121, 122, ..., 12n), the voltage having the level corresponding to the output is selected and outputted. In the display with a certain gray-scale, a voltage is outputted from the voltage selector during the first and second periods and in other gray-scale close to this gray-scale, voltages having varying adjoining levels are outputted alternately from the voltage selector (31, 32, ..., 3n) during the first and second periods.

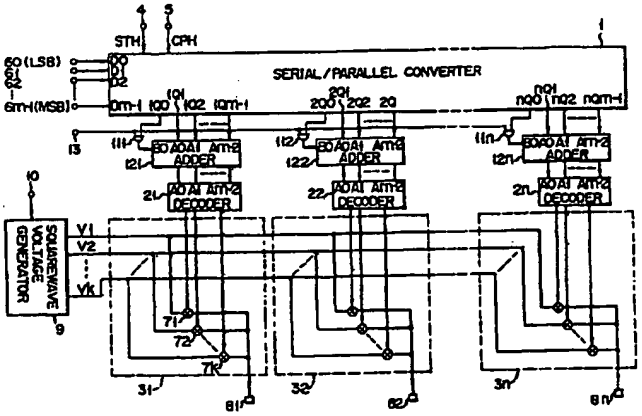


FIG. 4

EP 0 458 169 A2

The present invention relates to a drive circuit for active matrix type liquid crystal display device, and more specifically, to the drive circuit which drives the signal lines.

Recently, highly sophisticated active matrix type liquid crystal display devices have been developed, which are suited for personal computers and wrokstations. In this type of liquid crystal display device, signal lines and scanning lines are formed in the matrix in the liquid crystal panel and at the intersections, switch elements such as thin film transistors and pixel electrodes are formed. In this liquid crystal display element, the switch element is driven for every horizontal line by either ON or OFF signal and video signal voltage is fed selectively to the pixel electrode, exciting the liquid crystal held between the pixel electrode and the counter electrode, and the light passing the liquid crystal layer is modulated by the video signal voltage. As a result, multi-gray-scale or full-color images are displayed on the liquid crystal display device.

The video signal voltage from the outside is fed to the drive circuit which drives signal liens of the liquid crystal panel. This signal line drive circuit falls into two broad categories: analog type which uses analog video signals as input and digital type which uses digital video signals as input. In the analog type drive circuit, the video signal entered in series is successively sampled and held, converted into an analog parallel video signal which corresponds to one horizontal line, and outputted from the output terminal to drive the liquid crystal display device. In contrast, in the digital type drive circuit, the digital video signal is inputted and converted to an analog parallel video signal which corresponds to one horizontal line and is outputted from the output terminal. The drive circuit is formed with a D/A converter which converts digital signals to analog signals. One example of this digital type signal line drive circuit is that disclosed in Unexamined Patent Publication No. 63-161495.

Fig. 1 shows a conventional digital type signal line drive circuit, which consists of a serial parallel converter 1, plurality of decoders 21, 22, ... 2n, and voltage selectors 31, 32, ... 3n. The serial parallel converter 1, though its detailed circuit configuration is omitted, primarily consists of a shift register, latches and the like, as is well-known. In this serial parallel converter 1, to the input terminal 6, multi-gray-scale digital video signals, for example, video signals with m-bit gray-scale are inputted, while to the terminal 5, the shift clock CPH is inputted and to the terminal 4, the horizontal start signal STH is inputted. The video signals inputted in synchronism with the shift clock CPH are converted to parallel video data which correspond to the pixels in the liquid crystal panel by controls of the CPH and STH so that video signal voltages can be supplied simultaneously to the signal lines of the liquid crystal panel, and are supplied to decoders 21, 22, ..., 2n. At this point, the parallel video data with m-bit gray-scale are decoded by decoders 21, 22, ..., 2n and carry out ON-OFF-control for a large number of switches located inside the voltage selectors 31, 32, ..., 3n. To the voltage selectors 31, 32, ..., 3n, liquid crystal drive voltages V1, V2, ..., Vx are fed in common and either one of these drive voltages is selected according to the output of decoders 21, 22, ..., 2n and outputted to the output terminals 81, 82, ..., 8n. Because the liquid crystals panel must be driven with an alternate current, the number of liquid crystal driving voltages V1, V2, ..., Vx is $x = 2 \times 2^m$ when the voltages are supplied with direct current, and $x = 2^m$ when the voltages are supplied in square wave voltage form with two voltage levels. The input from terminal DF to decoders 21, 22. ..., 2n shown in Fig. 1 is used to supply liquid crystal voltage V1, V2, ..., Vx in direct current and is provided to deliver different decoding outputs even against the same gray-scale data input at a specified period, e.g., every frame period, so that it may correspond to the ac drive for liquid crystal.

In the conventional digital type signal line drive circuit, 2^m sorts of bi-level liquid crystal driving voltage are selected and outputted for the input digital video signals with m-bit gray-scale and fed to the liquid crystal panel. Corresponding to the pixels in the liquid crystal panel, for example, when the drive voltages outputted from this digital signal line drive circuit is fed to the color panel equipped with color filters comprising red, green, and blue, the number of colors to be displayed is $(2^m)^3$. More specifically, when a panel equipped with red, green, and blue color filters is driven with the 3-bit (8 gray-scale) digital video signals, 512 colors can be displayed.

In the conventional digital type signal line drive circuit, supposing that for example, in the case of m = 3 bits or 8 gray-scale display the number of levels of liquid crystal driving voltage are 8 each (V1P - V8P and V1N - V8N) above and below the counter electrode voltage VCOM of the liquid crystal panel as shown in Fig. 2 because the liquid crystal panel does not need an ac drive, and each level is fed alternately at a specified period, for example, every frame period T. Consequently, in this driving method, 16 levels are required, and the number of switches 7 for the voltage selector 31, 32, ... 3n is 16 when liquid crystal voltages V1, V2, ..., Vx are supplied with direct current and is 8 even in the case of bi-level square wave voltage.

As described above, in the conventional digital type signal line drive circuit, the number of switch 7, composing the voltage selector 31, 32, ..., 3n

must be, at least, as many as the number of gray-scale to be displayed. Consequently, the intention to increase the number of gray shades requires more switches and increases the chip size when the circuit is integrated into an LSI, producing a problem of high cost.

The objective of this invention is to provide a drive circuit for the active matrix liquid crystal display device, which can reduce the required switches for selecting liquid crystal driving voltages to about a half the number of gray-scale to be displayed in the digital type signal line drive circuit of the active matrix type liquid crystal display device. When integrating the drive circuit into an LSI, this invention can reduce the chip size greatly and can provided an inexpensive driver LSI.

According to this invention, an active matrix type liquid crystal display device comprises serial parallel conversion means for receiving digital video signals having m-bit gray-scale consisting of 2^0, 2^1, 2^2, ..., 2^{m-1} digits successively and converting them into parallel gray-scale corresponding to one line, modifying means for permitting the outputs of (m-1) bit gray-scale data excluding the least significant bit in accordance with this least significant bit of the m-bit parallel gray-scale data from the serial parallel conversion means during a first period and modifying the (m-1) bit gray-scale data in accordance with the least significant bit to permit the output of the modified (m-1) bit gray-scale data during a second period following the first period, decoding means for decoding the gray-scale data from the modifying means to output decoded data, voltage generating circuit for generating liquid crystal driving voltages having different levels each other, and voltage selectors for selecting one of the liquid crystal driving voltages from the voltage generating circuit in accordance with the decoded data, the voltage selectors continuously output one of the liquid crystal driving voltages during the first and second periods depending upon the decoded data, or the voltage selectors alternately output two of the liquid crystal driving voltages having adjoining levels during the first and second periods, respectively.

According to this invention, an active matrix type liquid crystal display device, comprising modifying means for receiving m-bit gray-scale digital video signals consisting of 2^0, 2^1, 2^2, ..., 2^{m-1} digits, permitting the outputs of (m-1) bit gray-scale digital video signals excluding the least significant bit of the m-bit gray-scale digital video signals in accordance with this least significant bit during a first period and modifying the (m-1) bit gray-scale digital video signals in accordance with this least significant bit of the m-bit gray-scale digital image signals to permit the output of the modified (m-1) bit gray-scale digital video signals during a second period following the first period, serial parallel conversion means for receiving digital video signals having (m-1) bit gray-scale from the modifying means successively and converting them into parallel gray-scale data corresponding to one line, decoding means for decoding the gray-scale data from the serial parallel conversion means to output decoded data, voltage generating circuit for generating liquid crystal driving voltages having different levels each other, and voltage selectors for selecting one of the liquid crystal driving voltages from the voltage generating circuit in accordance with the decoded data, the voltage selectors continuously output one of the liquid crystal driving voltages during the first and second periods depending upon the decoded data, or the voltage selectors alternately output two of the liquid crystal driving voltages having adjoining levels during the first and the second period.

In addition, according to this invention, a drive circuit for active matrix type liquid crystal display devices is provided.

According to this invention, because in the digital type signal line drive circuit, since a voltage selector is designed to select and alternately output two adjoining levels of liquid crystal driving voltages prepared beforehand during every first and second specified periods, the liquid crystal driving voltage with the intermediate level between the two levels is obtained as a result of time-average after the two voltages pass through a selection switch in the voltage selector. Consequently, the number of selection switches in the voltage selector can be reduced to about a haft the number of gray-scale to be displayed and an inexpensive driver LSI can be obtained.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing a conventional digital type signal line drive circuit for an active matrix type liquid crystal display device;

Fig. 2 is a graph showing the relationship between the number of gray-scale to be displayed and that of the liquid crystal driving voltage levels in a conventional drive circuit;

Fig. 3 is a plan schematically showing an active matrix type liquid crystal display device;

Fig. 4 is a block diagram showing a digital type signal line drive circuit for an active matrix type liquid crystal display device related to the first embodiment according to the present invention;

Figs. 5A to 5H and Fig. 6 are waveform diagrams explaining the operation of the drive circuit shown in Fig. 4;

Figs. 7A to 7D are waveform diagrams explaining the relationship between the operation in the

drive circuit shown in Fig. 4 and voltages fed to pixels from this drive circuit;

Fig. 8 is a block diagram showing a circuit related to a modified embodiment of the drive circuit shown in Fig. 4;

Fig. 9 is a block diagram showing a drive circuit for an active matrix type liquid crystal display device related to the second embodiment of the present invention;

Fig. 10 is a block diagram showing a circuit related to the modified embodiment of the drive circuit shown in Fig. 9;

Fig. 11 is a block diagram showing a drive circuit for an active matrix type liquid crystal display device related to the third embodiment of the present invention;

Fig. 12 is a voltage waveform diagram showing voltages supplied to the drive circuit shown in Fig. 11; and

Fig. 13 is a block diagram showing a circuit related to a modified embodiment of the drive circuit shown in Fig. 11.

Referring now to the drawings, the preferred embodiments of a drive circuit according to this invention for the active matrix type liquid crystal display device are explained in detail.

(First Embodiment)

In general, the active matrix type liquid crystal display device has the signal lines 202 and scanning lines 204 formed in matrix in the liquid crystal panel 200 as shown in Fig. 3 and has a pixel electrode 210 and a thin-film transistor 212 as a switch element formed at the intersections. In this liquid crystal display device, a row of the switch element 212 is driven by the ON/OFF signal corresponding to one horizontal line provided by the scanning line drive circuit 230 and the signal voltage supplied from the signal line drive circuit 220 to signal lines 202 is supplied selectively to the pixel electrode 210. The liquid crystal 216 held between the pixel electrode 210 corresponding to the switch element and the counter electrode 214 is, then, excited and the light passing the liquid crystal layer is modulated by the signal voltage, and as a result, an image having multi-gray-shade is displayed on the liquid crystal panel 200.

Fig. 4 shows a drive circuit for the active matrix type liquid crystal display device related to one embodiment according to this invention. This drive circuit consists of a serial parallel converter 1, decoders 21, 22, ..., 2n, and voltage selectors 32, 32, ..., 3n. To the serial parallel converter 1, an input terminal 4 to which the horizontal start signal STH is inputted, an input terminal 5 to which horizontal shift clock CPH is inputted, and input terminals 60, 61, ..., 6m-1 to which digital video signals having m-bit gray-scale are inputted are provided. In the voltage selectors 31, 32, ..., 3n, switches 71, 72, ..., 7k which are turned on or off by the input from the decoders 21, 22, ..., 2n are provided, and are connected not only to the output terminals 81, 82, ... 8n but also to the squarewave voltage generator 9 which generates squarewave voltage V1, V2, ..., Vk to drive the liquid crystal. To the squarewave generator, an input terminal 10, to which control signals to control the frequency of squarewave voltage V1, V2, ..., Vk is inputted, is provided. The AND circuits, that is, AND gates 111, 112, ..., 11n and binary full adders 121, 122, ..., 12n are connected between the serial parallel converter 1 and decoders 21, 22, ..., 2n, and the input terminal 13 to which an adding control signal is inputted is connected to AND gates 111, 112, ..., 11n.

Next, discussion will be made on the operation of the drive circuit shown in Fig. 4. The digital video signal having m-bit gray-scale consisting of 2^0, 2^1, 2^2, ..., 2^{m-1} digits are inputted to the serial parallel converter 1 via terminals 60, 61, 62, ..., 6m-1, and with the horizontal start signal STH and horizontal shift clock CPH inputted to the terminals 4 and 5, this video signal is serial-parallel-converted to the video data corresponding to one line successively, and the m-bit gray-scale parallel video data are outputted from the output terminals (1Q0, 1Q1, 1Q2, ..., 1Qm-1), (2Q0, 2Q1, 2Q2, ..., 2Qm-1), and (nQ0, nQ1, nQ2, ..., nQm-1), as shown in Fig. 5A to 5D, respectively.

Among these gray-scale data, the (m-1) bit gray-scale data excluding 2^0 digit (LSB) shown in Fig. 5B to 5D are supplied to the augend input terminals A0, A1, ..., Am-2 of the adders 121, 122, ..., 12n, while the 2^0 digit (LSB) data only is supplied to one of the input terminals of AND gates 111, 112, ..., 11n. To the input terminals of the other end of all AND gates, the adding control signal which reverses its polarity every specified period T1, e.g. a period of every 2 frames as shown in Fig. 5E, is supplied in common from the terminal 13. Consequently, from each AND gate, the 2^0 digit data shown in Fig. 5A is gated and outputted as sown in Fig. 5F only during the high level period of the adding control signal shown in Fig. 5E. The output signal shown in Fig. 5F is supplied to the addend input terminals B0 of adders 121, 122, ..., 12n. The output signal shown in Fig. 5F as the add end data is added to the (m-1) bit gray-scale data which is the augend data shown in Fig. 5B to 5D. Fig. 5G and 5H show the 2^1 and 2^2-digit data of the added outputs from the adder 121. Every other specified period T1, 1 LSB data is added to the (m-1) bit gray-scale data according to the contents of the 2^0 digit (LSB) data shown in Fig. 5A and the adding control signal shown in Fig. 5E. These adder outputs are supplied to the input

terminals A0, A1, ..., Am-2 of (m-1) bit decoders 21, 22, ..., 2n and are decoded, respectively, and are given to switches 71, 72, ..., 7k in the voltage selectors 31, 32. ..., 3n to ON/OFF control the switches 71, 72, ..., 7k. Then, liquid crystal driving voltages V1, V2, ..., Vk are supplied to the input side of the switches 71, 72, ..., 7k, from the squarewave voltage generator 9, the voltages corresponding to the decoder outputs are selected and outputted to the output terminals 81, 82, ..., 8n, respectively.

In this event, the squarewave voltages V1, V2, ..., Vk for during liquid crystal supplied to the input side of the switches 71, 72, ..., 7k take two levels each (V1P and V1N), (V2P and V2N), ..., (VkP and VkN) above and below the center voltage Vsc, common to each squarewave voltage, every specified period T2 as shown in Fig. 6. P and N suffix voltage levels are equal in the absolute value with reference to the center voltage Vsc. This specified period T2 is determined by the drive system of the liquid crystal display device, but it is preferable to be chosen the frame period or its integer multiples, or line period or its integer multiples. To the terminal 10 in Fig. 4, a signal to control T2 is supplied. The numbers (value of k) of the liquid crystal driving voltages V1, V2, ..., Vk and switches 71, 72, ..., 7k are determined by the number of gray-scale to be displayed, but when the drive circuit of this invention is employed, the k number may be reduced to half that in the case of conventional drive circuit, as will be described later. For example, when 15 gray-scale are displayed, eight liquid crystal driving voltages V1, V2, ..., V8 can be given and eight switches 71, 72, ..., 78 may be installed. That is, because the carry of the binary full adder is not inputted to the decoder, when the digital video signal having m-bit gray-scale is inputted, the image can be displayed with gray shades of 2^m-1, and in the voltage selector, only 2^{m-1} pieces of switch are required.

Referring now to Fig. 7A to 7D, the relationship between the liquid crystal driving voltages outputted from the output terminals 81, 82, ..., 8n of Fig. 4 and the number of gray shades is described.

Fig. 7A again shows the adding control signal shown in Fig. 5E, and the polarity of this signal is reversed every specified period T1, e.g. every two-frame period, as explained before. Fig. 7B again shows the 2^0 digit (LSB) data of the m-bit gray-scale video data shown in Fig. 5A. When 2^0 digit (LSB) data attains a high level (data "present") during the period of high level adding control signal, for example, during the period shown in τ in Fig. 7A, 1 LSB data is added to the input data to decoders 21, 22, ..., 2n in Fig. 4, and therefore, the voltage selectors 31, 32, ..., 3n select the liquid crystal driving voltage having one rank higher level. That is, as shown in Fig. 7C, when the 2^0 digit data, shown in Fig. 7B, in the video data is at the low level (data "absent"), assuming that the liquid crystal driving voltage V1P and V1N are supplied to a pixel alternately every specified period, e.g. one frame period. When the 2^0 digit data shown in Fig. 7B attains the high level (data "present"), there is no change in the liquid crystal driving voltage while the adding control signal shown in Fig. 7A is at the low level, but during the high level period, the liquid crystal driving voltage having one rank higher level V2P and V2N is supplied. To explain this for an optional pixel, when the 2^0 digit data shown in Fig. 7B is at the low level (data "absent"), the liquid crystal driving voltage ViP and ViN are supplied while the adding control signal shown in Fig. 7A is at the low level, if the 2^0 digit data shown in Fig. 7B becomes at the high level (data "present"), V(i+1)P and V(i+1)N are supplied every high level period of the adding control signal shown in Fig. A ($0 \leq i \leq k-1$). That is, depending on presence or absence of the 2^0 digit data shown in Fig. 7B, the liquid crystal driving voltage supplied to the pixel is controlled to two types of level. Consequently, in the drive circuit shown in Fig. 4, the second voltages V2, ..., Vk with higher level is added to either one of the first liquid crystal driving voltages V1, V2, ..., Vk-1 by the control of switches 71, 72, ..., 7k, and if averaged by time, nearly intermediate voltage between these two voltages can be supplied to the pixel of the liquid crystal display device. Now supposing the k be 8, it is possible to supply 15 (2k-1) types of drive voltage comprising eight voltages V1-V8 determined by the k plus seven (k-1) intermediate voltages to the pixel of the liquid crystal display device, enabling the display of 15 gray shades.

Fig. 8 shows a drive circuit related to a modified embodiment of the first embodiment according to the present invention. The difference between the circuit shown in Fig. 8 and that in Fig. 4 is that the circuit is simplified by providing the AND gate (11) and the adder (12) on the input side of the serial parallel converter (1) so that only one each circuit is required. In Fig. 8, the circuit elements corresponding to Fig. 4 are given the same number. That is, the numeral 1 is a serial parallel converter, 11 an AND gate, 12 a binary full adder, 13 an adding control signal input terminal, and 60, 61, 62, ..., 6m-1 m-bit gray-scale digital video signal input terminals. Other portions are same as in Fig. 1 and explanation is omitted.

In the drive circuit shown in Fig. 8, when the digital video signal having m-bit gray-scale consisting of 2^0, 2^1, 2^2, ..., 2^{m-1} digits is supplied from the terminals 60, 61, 62, ..., 6m-1, the (m-1) bit gray-scale digital video signal excluding the 2^0 digit is supplied to the augend data input terminals A0, A1,

..., Am-2 of the adder 12 and the 2^0 digit (LSB) digital video signal is supplied to one of the input terminals of the AND gate 11. To the other input terminals of the AND gate 11, the adding control signal shown in Fig. 5E is supplied from the terminals 13. While this adding control signal is at high level, the 2^0 digit (LSB) digital signal is gated and supplied to the added data input terminal B0 of the adder 12. If the data of the terminals B0 is at high level, the 1 LSB data is added to the (m-1) bit gray-scale digital video signal supplied to the augend data input terminals A0, A1, ..., Am-2. The added output is supplied to the input terminals D0, D1, ..., Dm-2 of the serial parallel converter 1 and serial-parallel converted every one line by the control implemented by the horizontal start signal STH and horizontal shift clock CPH inputted from the terminals 4 and 5. The operation thereafter is similar to that described in the previous embodiment.

In this modified embodiment, providing the binary full adder 12, and AND gate 11 on the input side of the serial parallel converter 1 can simplify the drive circuit. In this event, the serial parallel converter 1 and decoders 21, 22, ..., 2n are both only required to process (m-1) bits for m-bit gray-scale digital video signal and can utilize conventional IC elements for drive. That is, only adding some circuits to conventionally used IC elements for drive can greatly increase the number of gray shades to be displayed. According to this invention, the number of switches required for selecting liquid crystal driving voltages can be reduced to half the number of gray shades to be displayed in the digitally constituted signal line drive circuit for the active matrix type liquid crystal display device. Accordingly, when integrating the drive circuit into an LSI, the chip size can be greatly reduced and an inexpoensive drive LSI can be provided.

(Second Embodiment)

In the first embodiment according to the invention, it is limited that only the (2^m-1) gray-scale can be displayed, even if the digital video data having m-bit gray-scale is inputted into the drive circuit shown in Figs. 4 and 8. Thus, it is required that the digital video data is so processed by the external circuit, i.e., a bit pattern, generator as to exclude one of the bit patterns, which can not be displayed, from the digital video data. That is, in the driver related to the first embodiment, two liquid crystal drive voltages with not adjacent levels, that is, voltage Vk and voltage V1 shown in Fig. 6, are selected alternately and outputted, and it is necessary to prevent in advance generation of the bit pattern, which is unable to display, on the external circuit side. This can be prevented by the driver related to the second embodiment. The signal line drive circuit for the active matrix type liquid crystal display device related to the second embodiment is shown in Fig. 9. The circuit shown in Fig. 9 has a different circuit arrangement in which AND gate 141, 142, ... 14n and NAND gates 151, 152, ... 15n are provided between a serial parallel converter 1 and AND gates 111, 112, ... 11n, as that in Figs. 4 and 8. In Fig. 9, the same numbers are given to the same portions shown in Fig. 4 and 8. That is, numerals 21, 22, ..., 2n are decoders, 31, 32, ..., 3n voltage selectors, 4 a horizontal start signal STH input terminal, 5 a horizontal shift clock CPH input terminal, 60, 61, 62, ..., 6m-1 m-bit gray-scale digital video signal input terminals, 71, 72, ..., 7n, switches, 81, 82, ..., 8n output terminals, 9 a liquid crystal driving squarewave voltage generator, V1, V2, ..., Vk liquid crystal driving voltage generating outputs, 10 an input terminal for squarewave voltage frequency control signal, 121, 122, ..., 12n binary full adders, and 13 input terminals for adding control signal.

Next, discussion will be made on the operation of the drive circuit according to the second embodiment.

In the drive circuit shown in Fig. 9, the digital video signal having m-bit gray-scale consisting of 2^0, 2^1, 2^2, ..., 2^{m-1} digits are inputted to the serial parallel converter 1 via terminals 60, 61, 62, ..., 6m-1, and with the horizontal start signal STH and horizontal shift clock CPH inputted to the terminals 4 and 5, this video signal is serial-parallel-converted for every one line and outputted to the output terminals (1Q0, 1Q1, 1Q2, ..., 1Qm-1), (2Q0, 2Q1, 2Q2, ..., 2Qm-1), and (nQ0, NQ1, nQ2, ..., nQm-1). These output signals correspond to the m-bit gray-scale parallel video data are the same as shown in Fig. 5A to 5D. Of these gray-scale data, the (m-1) bit gray-scale data excluding 2^0 digit (LSB) shown in Fig. 5A is supplied to the input terminals A0 A1, ..., Am-2 of the adders 121, 122, ..., 12n and input terminals of NAND gates 151, 152, ..., 15n, while the 2^0 digit (LSB) data only is supplied to one of the input terminals of AND gates 141, 142, ..., 14n. Outputs of NAND gates 151, 152, ..., 15n are inputted to other input terminals of AND gates 141, 142, ..., 14n. If the (m-1) bit gray-scale data excluding the 2^0 digit (LSB) data is the maximum, the output level of the AND gates 141, 142, ..., 14n becomes low irrespective of the 2^0 digit data content. This output of AND gates 141, 142, ..., 14n is inputted to one of the input terminals of the AND gates 111, 112, ..., 11n, respectively. To the other input terminals, the adding control signal which reverses its polarity every specified period T1, e.g. a period of every 2 frames as shown in Fig. 5E, is supplied in common from the terminals 13. Consequently, in each of the AND gates 111, 112, ..., 11n, the 2^0 digit data shown in Fig. 5A is gated and outputted as shown in Fig. 5F only during the high level period of the adding control

signal shown in Fig. 5E.

The output signal shown in Fig. 5F is supplied to the addend data input terminal B0 of adders 121, 122, ..., 12n and added to the (m-1) bit gray-scale data of Fig. 5B to 5D supplied to the augend data input terminals A0, A1, ..., Am-2. Fig. 5G and 5H show the 2^1 and 2^2-digit signals of the added outputs. Same as the first embodiment already described, every specified period T1, 1 LSB data is added to the (m-1) bit gray-scale data according to the contents of the 2^0 digit data. These added outputs are supplied to the input terminals A0, A1, ..., Am-2 of (m-1) bit decoders 21, 22, ..., 2n and are decoded, respectively, and ON-OFF control the switches 71, 72, ..., 7k in the voltage selectors 31, 32, ..., 3n. Then, from the squarewave voltage generator 9 supplied to the input side of the switches 71, 72, ..., 7k, either one of voltages V1, V2, ..., Vk, which matches the decoder outputs, is selected and outputted from the output terminals 81, 82, ..., 8n, respectively.

The relationship between the liquid crystal driving voltage outputted from the output terminals 81, 82, ..., 8n of Fig. 9 and the number of gray-scale is the same as that described referring to Fig. 7A to 7D in the first embodiment and therefore the description is omitted.

In the drive circuit shown in Fig. 9, when the (m-1) bit gray-scale data supplied to the augend input terminals A0, A1, ..., Am-2 of the binary full adders 121, 122, ..., 12n is the maximum, the AND gate 141, 142, ..., 14n are closed by the NAND gates 151, 152, ..., 15n, and addition of 1LSB data for every specified period is stopped even if the 2^0 digit data becomes high level. This can prevent alternate selection and output of two liquid crystal driving voltages whose levels are not adjacent each other, that is, voltage Vk and V1 shown in Fig. 6. Consequently, the liquid crystal display device becomes capable for receiving all the types of bit patterns as m-bit gray-scale data and it is no longer necessary to prevent in advance the generation of the bit pattern, which cannot be displayed, on the outside circuit which generates the m-bit gray-scale data.

Fig. 10 shows a drive circuit related to a modified embodiment of the second embodiment according to the present invention and has a circuit configuration similar to the circuit shown in Fig. 8. In Fig. 10, the circuit elements corresponding to the first and the second embodiments are given the same number. That is, the numeral 1 is a serial parallel converter, 11 an AND gate, 12 a binary full adder, 13 an adding control signal input terminals, and 60, 61, 62, ..., 6m-1 m-bit gray-scale digital video signal input terminals.

In the drive circuit related to this modified embodiment, even if the digital video signal with m-bit gray-scale is inputted, a serial parallel converter which can process (m-1) bit gray-scale can be employed. In addition, it has a feature that only one circuit each of the AND gate 11 and 14 and NAND gate 15 and adder 12 is required.

Now the operation of the drive circuit related to the modified embodiment shown in Fig. 10 is described.

In the drive circuit shown in Fig. 10, when the digital video signal having m-bit gray-scale consisting of 2^0, 2^1, 2^2, ..., 2^{m-1} digits is supplied from the terminals 60, 61, 62, ..., 6m-1, the (m-1) bit gray-scale digital video signal excluding the 2^0 digit is supplied to the augend data input terminals A0, A1, ..., Am-2 of the adder 12 and to input terminals of NAND gate 15. The output of the NAND gate 15 is led to one of the input terminals of the AND gate 14, and to the other input terminals of the AND gate 14, the 2^0 digit (LSB) signal is supplied. The output of the AND gate 14 is supplied to one of the input terminals of the AND gate 11 and to the other input terminals of the AND gate 11, the adding control signal shown in Fig. 5E is supplied from the terminal 13. While this adding control signal is at high level, the 2^0 digit (LSB) video signal is gated and supplied to the addend data input terminals B0 of the adder 12. If the data on the terminal B0 is at high level, 1LSB data is added to the digital video signal with (m-1) bit gray-scale supplied to augend input terminals A0, A1, ..., Am-2 of the adder 12. The added outputs are supplied to the input terminal D0, D1, ..., Dm-2 of the serial parallel converter 1 and serial-parallel converted every one line by the control implemented by the horizontal start signal STH and horizontal shift clock CPH inputted from the terminals 4 and 5. This serial-parallel converted outputs are supplied to the input terminals A0, A1, ..., Am-2 of the (m-1) bit decoders 21, 22, 2n, and are decoded, and ON-OFF control the switches 71, 72, ..., 7k in the voltage selectors 31, 32, ..., 3n. Then, from the squarewave voltage generator 9 supplied to the input side of the switches 71, 72, ..., 7k, either one of voltages V1, V2, ..., Vk, which matches the decoder outputs, is selected and outputted from the output terminals 81, 82, ..., 8n, respectively.

In this event, when the digital video signal having the (m-1) bit gray-scale is the maximum, the AND gate 14 is closed by the NAND gate 15, and addition of the 1LSB data is stopped even if the the 2^0 digit data is high. This configuration can prevent the case in which two liquid crystal driving voltages with no adjacent levels, that is, the case in which Vk and V1 of Fig. 6 are alternately selected and outputted.

In this modified embodiment, providing the binary full adder 12, AND gates 11 and 14 and NAND gate 15 on the input side of the serial

parallel converter 1 can simplify the drive circuit. In this event, the serial parallel converter 1 and decoders 21, 22, ..., 2n are both only required to process (m-1) bits and can utilize conventional IC elements for drive. That is, only adding some circuits to conventionally used IC elements for drive can greatly increase the number of gray shades to be displayed.

In the first and second embodiments, binary full adders are employed, but the present invention shall not be limited to these but the same effect can be obtained by carrying out subtraction with subtractors in place of carrying out addition in each embodiment. In this event, when the (m-1) bit gray-scale digital video signal which serves as the minuend data is the minimum, a gate circuit to stop subtraction of 1LSB is added to the subtractor. It is possible to combine with other logic circuit such as latch. (Third Embodiment)

In the drive circuits related to the first and the second embodiments, inputs of the m-bit gray-scale digital video signal are received but only 2^m-1 gray shades can be displayed, but according to the third embodiment, 2^m gray shades can be selected and displayed. Fig. 11 shows the drive circuit which includes only one more switches (7t+1) in comparison with the circuit shown in Fig. 4, according to the third embodiment of this invention. In Fig. 11, numeral 1 is a serial parallel converter, 21, 22, ..., 2n decoders, 31, 32, ..., 3n voltage selectors, 4 a horizontal start signal STH input terminal, 5 a horizontal shift clock CPH input terminal, 60, 61, 62, ..., 6m-1 input terminals for digital video signal with m-bit gray-scale, 71, 72, ..., 7k, 7k+1 switches, 81, 82, ..., 8n output terminals, 9 a squarewave voltage generator for driving the liquid crystal, V1, V2, ..., Vk, Vk+1 voltage generator outputs for liquid crystal drive, 10 an input terminal for squarewave voltage frequency control signal, 111, 112, ..., 11n AND gates, 121, 122, ..., 12n binary full adders, 13 an input terminal for adding control signal.

Next, discussion will be made on the operation of the drive circuit according to the third embodiment. Almost all of the operations are similar to those described in the first and the second embodiments and explanation overlaps, but are described as follows.

In the drive circuit shown in Fig. 11, the digital video signal having m-bit gray-scale consisting of 2^0, 2^1, 2^2, ..., 2^{m-1} digits are inputted to the serial parallel converter 1 via terminals 60, 61, 62, ..., 6m-1, and with the horizontal start signal STH and horizontal shift clock CPH inputted to the terminals 4 and 5, this video signal is serial-parallel-converted for every one line and outputted to the output terminals (1Q0, 1Q1, 1Q2, ..., 1Qm-1), (2Q0, 2Q1, 2Q2, ..., 2Qm-1), and (nQ0, nQ1, nQ2, ..., nQm-1). This output signal corresponds to the m-bit gray-scale parallel video data converted in accordance with the m-bit gray-scale digital video signals as shown in Fig. 5A to 5D.

Of these parallel video data, the (m-1) bit gray-scale data excluding 2^0 digit (LSB) shown in Fig. 5A is supplied to the augend input terminals A0, A1, ..., Am-2 of the adders 121, 122, ..., 12n, while the 2^0 digit (LSB) data only is supplied to one of the input terminals of AND gates 111, 112, ..., 11n. To the other input terminal, the adding control signal which reverses its polarity every specified period T1, e.g., a period of every 2 frames as shown in Fig. 5E, is supplied in common from the terminal 13. Consequently, in each of the AND gates 111, 112, ..., 11n, the 2^0 digit data shown in Fig. 5A is gated and outputted as shown in Fig. 5F only during the high level period of the adding control signal shown in Fig. 5E.

The output signal shown in Fig. 5F is supplied to the adding data input terminal B0 of adders 121, 122, ..., 12n and added to the (m-1) bit gray-scale data of Fig. 5B to 5D supplied to the augend data input terminals A0, A1, ..., Am-2 as data of 1LSB. In this event, if the (m-1) bit gray-scale data shown in Fig. 5B-5D is the maximum, the carry data is outputted to the carry terminal Cm-2 of adders 121, 122, ..., 12n as added results of the 1 LSB data. The added result data comprising these (m-1) bit gray-scale data and 1-bit carry data is supplied to the input terminals A0, A1, ..., Am-1 of m bit decoders 21, 22, ..., 2n and are decoded, and ON/OFF control the switches 71, 72, ..., 7k, 7k+1 in the voltage selectors 31, 32, ..., 3n. Then, from the squarewave voltage generator 9 supplied to the input side of the switches 71, 72, ..., 7k, 7k+1, either one of voltages V1, V2, ..., Vk, Vk+1, which matches the decoder outputs, is selected and outputted from the output terminals 81, 82, ..., 8n, respectively.

The squarewave voltages V1, V2, ..., Vk, Vk+1 for driving liquid crystal supplied to the input side of the switches 71, 72, ..., 7k, 7k+1 take two levels each (V1P and V1N), (V2P and V2N), ..., (VkP and VkN), (Vk+1 P and Vk+1 N) above and below the center voltage Vsc, common to each squarewave voltage, every specified period T2, as shown in Fig. 12. P and N suffix voltage levels are equal in the absolute value with reference to the center voltage Vsc. The numbers of the liquid crystal driving voltages V1, V2, ..., Vk, Vk+1 and switches 71, 72, ..., 7k, 7k+1 are determined by the decoded number (k) for (m-1) bit plus one for m-bit gray-scale video signal as reference. For example, it is 5 for the 3-bit gray-scale (8 gray shades) video signal and 9 for the 4-bit gray-scale (16 gray shades) video signal. That is, in the circuit related to the third embodiment, it is only required to provide liquid

crystal driving voltages and switches in the number half that of the gray-scale to be displayed plus one.

The relationship between the drive output voltages outputted from the output terminals 81, 82, ..., 8n of Fig. 11 and the number of gray-scale is the same as that described referring to Fig. 7A to 7D in the first embodiment and therefore the description is omitted.

In the drive circuit shown in Fig. 11, a switch 7k+1 is provided in addition to switches 71, 72, ..., 7k and as shown in Fig. 12, the liquid crystal driving voltage Vk+1 is generated in addition to liquid voltages V1, V2, ..., Vk, and k pieces of voltage equivalent to nearly intermediate voltage of these voltages V1, V2, ..., Vk, Vk+1 can be supplied to pixels of the liquid crystal display device in addition to (k+1) pieces of voltages V1, V2, ..., Vk, Vk+1, when averaged by time. For example, providing 9 pieces each of switch and liquid crystal driving voltage permits the display of 17 gray shades. That is, in the first and second embodiments, 2^m-1 gray shades can be selected even though they receive the input of m-bit gray-scale digital video signals, but according to this third embodiment, 2^m gray shades can be selected.

Fig. 13 shows a modified embodiment of the drive circuit shown in Fig. 11. In the circuit related to this modified embodiment, a binary full adder 12 is provided on the input side of the serial parallel converter 1 as shown in Fig. 8 and Fig. 10 to simplify the circuit. This configuration permits installation of only one circuit each of AND gate 11 and binary full adder 12. Other circuit configuration is the same as that related to third embodiment shown in Fig. 11 and the explanation is omitted.

Now the operation of this embodiment is described referring Fig. 2 which is used in describing the operation of the first embodiment.

In the drive circuit shown in Fig. 13, when the digital video signal having m-bit gray-scale consisting of 2^0, 2^1, 2^2, ..., 2^{m-1} digits is supplied form the terminal 60, 61, 62, ..., 6m-1, the (m-1) bit gray-scale digital video signal excluding the 2^0 digit is supplied to the augend data input terminals A0, A1, ..., Am-2 of the adder 12. The 2^0 digit (LSB) signal is supplied to one of the input terminals of the AND gate 11. To the other side of the input terminals of the AND gate 11, the adding control signal shown in Fig. 5E is supplied form the terminal 13. While this adding control signal is at high level, the 2^0 digit (LSB) video signal is gated and supplied to the addend data input terminal B0 of the adder 12. When the level of the data on the terminal B0 is high, the data of 1LSB is added to the (m-1) bit gray-scale digital video signal supplied to the augend data input terminals A0, A1, ..., Am-2. In this event, if the aforementioned (m-1) bit gray-scale digital video signal is the maximum, the carry data is outputted to the carry terminal Cm-2 of the adder 12 as an added results of the 1 LSB data. The added results comprising these (m-1) bit gray-scale digital video signal and 1 bit carry data is supplied to the input terminals D0, D1, ..., Dm-1 of the serial parallel converter 1 and serial-parallel converted to make the parallel gray-scale data for every one line by the control implemented by the horizontal start signal STH and horizontal shift clock CPH inputted form the terminals 4 and 5. These gray-scale data are supplied to m-bit decoders 21, 22, ..., 2n, respectively and are decoded. The operation thereafter is the same as that of the third embodiment already described and the explanation is omitted.

In the above-mentioned embodiments, binary full adders are employed for data processing, but the present invention shall not be limited to these but the same effect can be obtained by carrying out subtraction with subtractors in place of carrying out addition. In this event, when the (m-1) bit minuend data is the minium, the borrow data is outputted from the subtractor as the subtracted results of 1LSB. The subtracted data comprising this 1-bit borrow data and (m-1) bit gray-scale data should be supplied to either serial parallel converter 1 or decoders 21, 22, ..., 2n. In this event, the amplitude of squarewave voltage Vk+1 for driving the liquid crystal of Fig. 6 or 12 can be set to be smaller than that of the squarewave voltage V1 of the same figures.

According to this invention, in the digitally constituted signal line drive circuit for the active matrix type liquid crystal display device, the required quantity of switches for selecting liquid crystal driving voltage can be reduced to nearly half that of the gray-scale to be displayed. When integrating the drive circuit into an LSI, this invention can reduce the chip size greatly and can provide an inexpensive driver LSI.

Claims

1. An active matrix type liquid crystal display device, characterized by comprising:

serial parallel conversion means (1) for receiving digital video signals having m-bit gray-scale consisting of 2^0, 2^1, 2^2, ..., 2^{m-1} digits successively and converting them into parallel gray-scale corresponding to one line;

modifying means (121, 122, ..., 12n) for permitting the outputs of (m-1) bit gray-scale data excluding the least significant bit in accordance with this least significant bit of the m-bit parallel gray-scale data from the serial parallel conversion means (1) during a first period and modifying the (m-1) bit gray-scale data in accordance with said least significant bit to per-

mit the output of the modified (m-1) bit gray-scale data during a second period following said first period;

decoding means (21, 22, ..., 2n) for decoding the gray-scale data from the modifying means (121, 122, ..., 12n) to output decoded data;

voltage generating circuit (9) for generating liquid crystal driving voltages having different levels each other; and

voltage selectors (31, 32, ..., 3n) for selecting one of the liquid crystal driving voltages from said voltage generating circuit (9) in accordance with the decoded data, said voltage selectors (31, 32, ..., 3n) continuously output one of the liquid crystal driving voltages during said first and second periods depending upon the decoded data, or said voltage selectors (31, 32, ..., 3n) alternately output two of the liquid crystal driving voltages having adjoining levels during said first and second periods, respectively.

2. An active matrix type liquid crystal display device according to claim 1, characterized in that the modifying means (121, 122, ..., 12n) includes an adding means (121, 122, ..., 12n) which adds the least significant bit data to the (m-1) bit gray-scale data excluding the least significant bit every said second period and outputs as modified data.

3. An active matrix type liquid crystal display device according to claim 1, characterized in that the modifying means (121, 122, ..., 12n) includes logic elements which permit outputs in accordance with the least significant bit and a modifying control signal during said second period.

4. An active matrix type liquid crystal display device according to claim 1, characterized in that the modifying means (121, 122, ..., 12n) includes means (121, 122, ..., 12n) for permitting outputs of the (m-1) bit gray-scale data during said first and second periods as long as the (m-1) bit gray-scale data are either the maximum or the minimum.

5. An active matrix type liquid crystal display device according to claim 4, characterized in that the modifying means (121, 122, ..., 12n) includes logic elements (111, 141, 151) which determine whether the (m-1) bit gray-scale data are the maximum or the minimum.

6. An active matrix type liquid crystal display device according to claim 1, characterized in that the voltage generating circuit (9) generates the liquid crystal driving voltages in the number equivalent to decoded number for (m-1) bit.

7. An active matrix type liquid crystal display device according to claim 1, characterized in that the voltage selector (31, 32, ..., 3n) generates the liquid crystal driving voltages in the number equivalent to decoded number for (m-1) bit plus one.

8. An active matrix type liquid crystal display device according to claim 1, characterized in that the voltage selectors (31, 32, ..., 3n) include switching elements (71, 72, ..., 7k) in the number equivalent to decoded number for (m-1) bit and each of the switching elements (71, 72, ..., 7k) is opened and closed by the decoded data from the decoding means (21, 22, ..., 2n).

9. An active matrix type liquid crystal display device according to claim 1, characterized in that the voltage selectors (31, 32, ..., 3n) include switching elements (71, 72, ..., 7k) in the number equivalent to decoded number for (m-1) bit plus one and each of the switching elements (71, 72, ..., 7k) is opened and closed by the decoded data from the decoding means (21, 22, ..., 2n).

10. An active matrix type liquid crystal display device according to claim 1, characterized in that the modifying means (121, 122, ..., 12n) generates the operation data comprising the (m-1) bit gray-scale digital pixel data and the 1-bit carry or borrow data.

11. An active matrix type liquid crystal display device, characterized by comprising:

modifying means (12) for receiving m-bit gray-scale digital video signals consisting of 2^0, 2^1, 2^2, ..., 2^{m-1} digits, permitting the outputs of (m-1) bit gray-scale digital video signals excluding the least significant bit of the m-bit gray-scale digital video signals in accordance with this least significant bit during a first period and modifying the (m-1) bit gray-scale digital video signals in accordance with this least significant bit of the m-bit gray-scale digital image signals to permit the output of the modified (m-1) bit gray-scale digital video signals during a second period following said first period;

serial parallel conversion means (1) for receiving digital video signals having (m-1) bit gray-scale from the modifying means (12) suc-

cessively and converting them into parallel gray-scale data corresponding to one line;

decoding means (21, 22, ..., 2n) for decoding the gray-scale data from the serial parallel conversion means (1) to output decoded data;

voltage generating circuit (9) for generating liquid crystal driving voltages having different levels each other; and

voltage selectors (31, 32, ..., 3n) for selecting one of the liquid crystal driving voltages from the voltage generating circuit (9) in accordance with the decoded data, said voltage selectors (31, 32, ..., 3n) continuously output one of the liquid crystal driving voltages during said first and second periods depending upon the decoded data, or said voltage selectors (31, 32, ..., 3n) alternately output two of the liquid crystal driving voltages having adjoining levels during said first and said second period.

12. An active matrix type liquid crystal display device according to claim 11, characterized in that the modifying means (12) includes an adding means (12) which adds the least significant bit data to the (m-1) bit gray-scale digital video signals excluding the least significant bit every said second period and outputs as modified output video signals.

13. An active matrix type liquid crystal display device according to claim 11, characterized in that the modifying means (12) includes at least one logic element (11, 14, 15) which permits outputs in accordance with the least significant bit and modifying control signal during said second period.

14. An active matrix type liquid crystal display device according to claim 11, characterized in that the modifying means (12) includes means (12) for permitting outputs of the (m-1) bit gray-scale digital video signals during said first and second periods as long as the (m-1) bit gray-scale digital video signal are either the maximum or the minimum.

15. An active matrix type liquid crystal display device according to claim 14, characterized in that the modifying means (12) includes a logic element (11, 14, 15) which determines whether the (m-1) bit gray-scale digital video signals are the maximum or the minimum.

16. An active matrix type liquid crystal display device according to claim 11, characterized in that the voltage generating circuit (9) generates the liquid crystal driving voltages in the number equivalent to decoded number for (m-1) bit.

17. An active matrix type liquid crystal display device according to claim 11, characterized in that the voltage generating circuit (9) generates the liquid crystal driving voltages in the number equivalent to decoded number for (m-1) bit plus one.

18. An active matrix type liquid crystal display device according to claim 11, characterized in that the voltage selectors (31, 32, ..., 3n) include switching elements (71, 72, ..., 7k) in the number equivalent to decoded number for (m-1) bit and each of the switching elements (71, 72, ..., 7k) is opened and closed by the decoded data from the decoding means (21, 22, ..., 2n).

19. An active matrix type liquid crystal display device according to claim 11, characterized in that the voltage selectors (31, 32, ..., 3n) include the switching elements (71, 72, ..., 7k) in the number equivalent to decoded number for (m-1) bit plus one and each of the switching element (71, 72, ..., 7k) is opened and closed by the decoded data from the decoding means.

20. An active matrix type liquid crystal display device according to claim 11, characterized in that the modifying means (12) generates the operation data comprising the (m-1) bit gray-scale digital video signals and the 1-bit carry or borrow data.

21. An active matrix type liquid crystal display device, characterized by comprising:

a receiving means (1, 12, 121, 122, ..., 12n, 111, 112, 11n) for receiving digital video signals having a plurality of gray-scale bits, and

a selecting means (31, 32, ..., 3n) for selecting one of a plurality of liquid crystal driving voltages and supplying it to pixels,

wherein a gray-scale number on the pixels is smaller than the theoretical gray-scale number for the digital video signals.

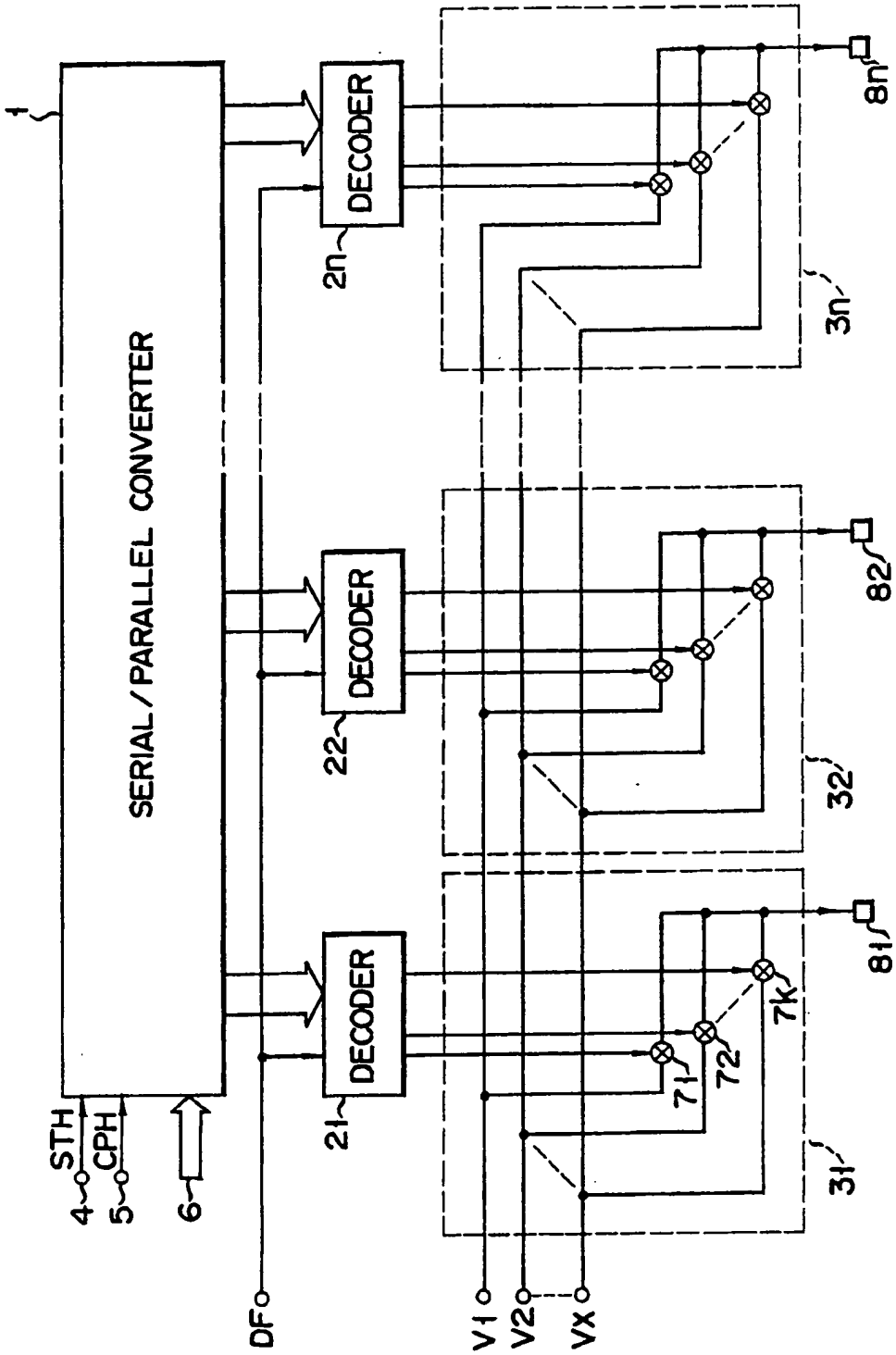
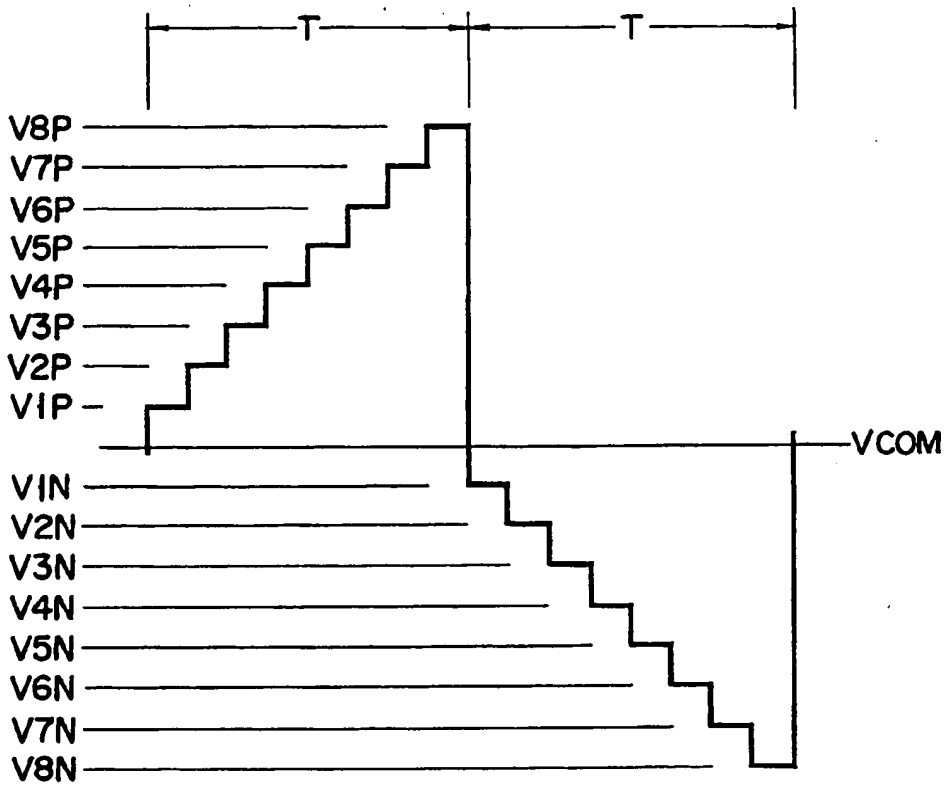

SERIAL / PARALLEL CONVERTER
DECODER
DECODER
DECODER
STH
CPH
DF
V1
V2
VX
1
2n
22
21
3n
32
31
8n
82
81
71
72
7k
4
5
6

FIG. 1


T
T
V8P
V7P
V6P
V5P
V4P
V3P
V2P
V1P
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V1N
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V3N
V4N
V5N
V6N
V7N
V8N

FIG. 2

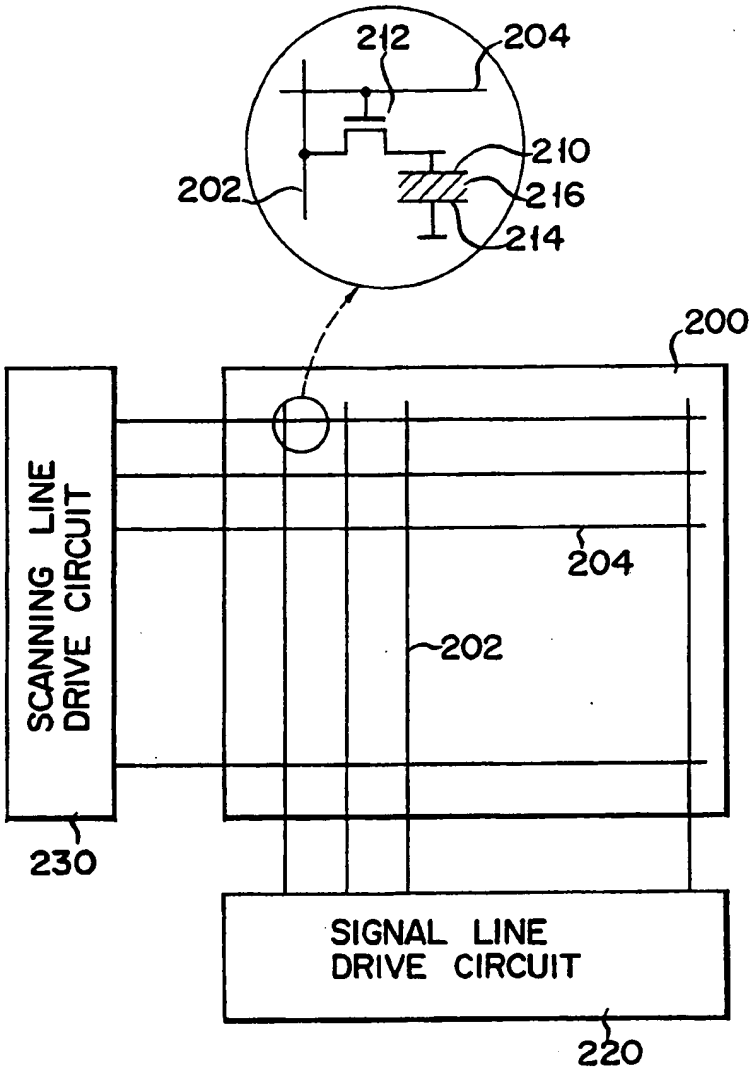
212
204
210
202
216
214
200
SCANNING LINE
DRIVE CIRCUIT
204
202
230
SIGNAL LINE
DRIVE CIRCUIT
220

FIG. 3

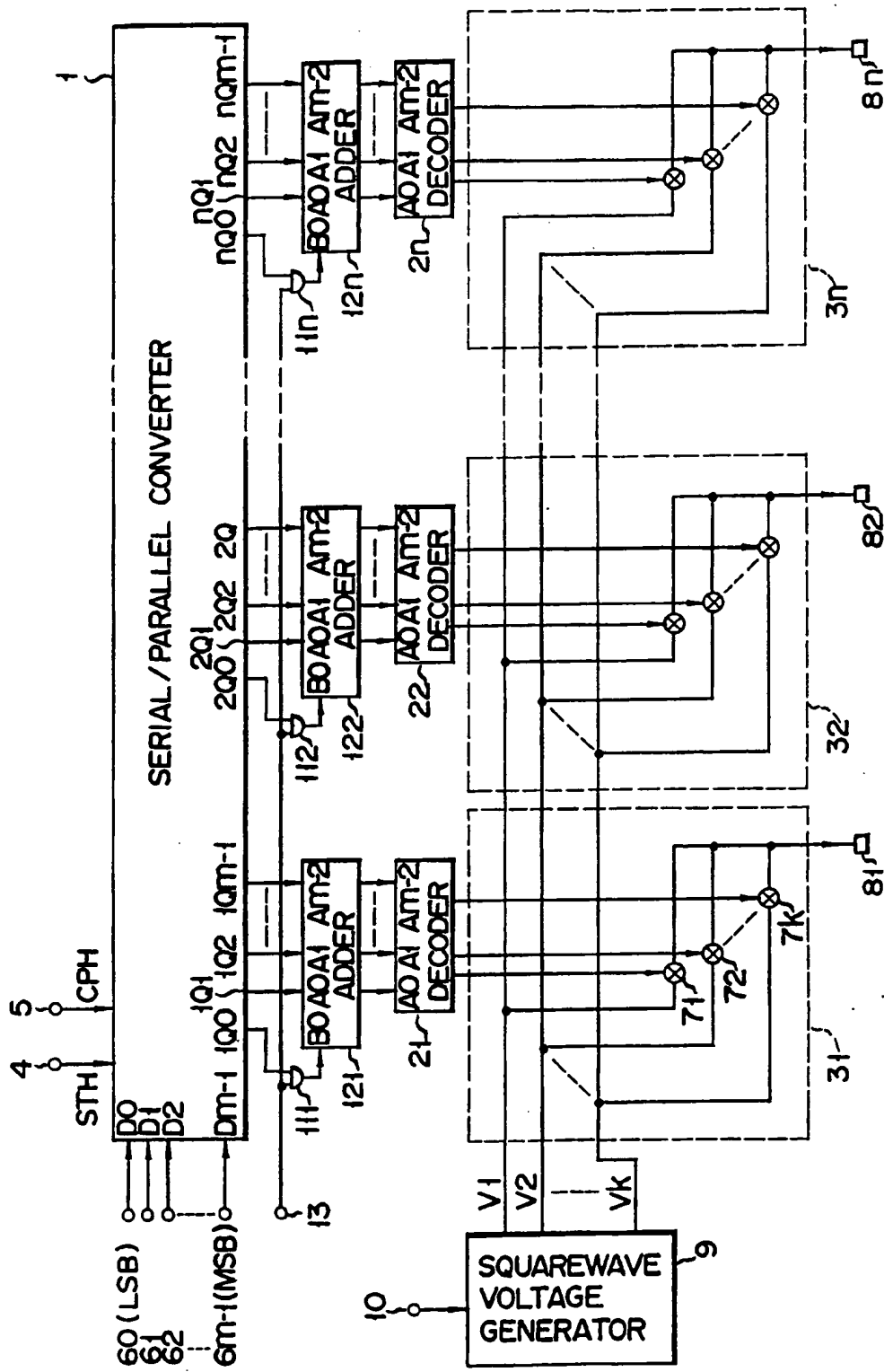
SERIAL/PARALLEL CONVERTER
STH
CPH
D0
D1
D2
Dm-1
BO
AO A1 Am-2
ADDER
AO A1 Am-2
DECODER
SQUAREWAVE VOLTAGE GENERATOR
V1
V2
Vk
60 (LSB)
61
62
6m-1 (MSB)

FIG. 4

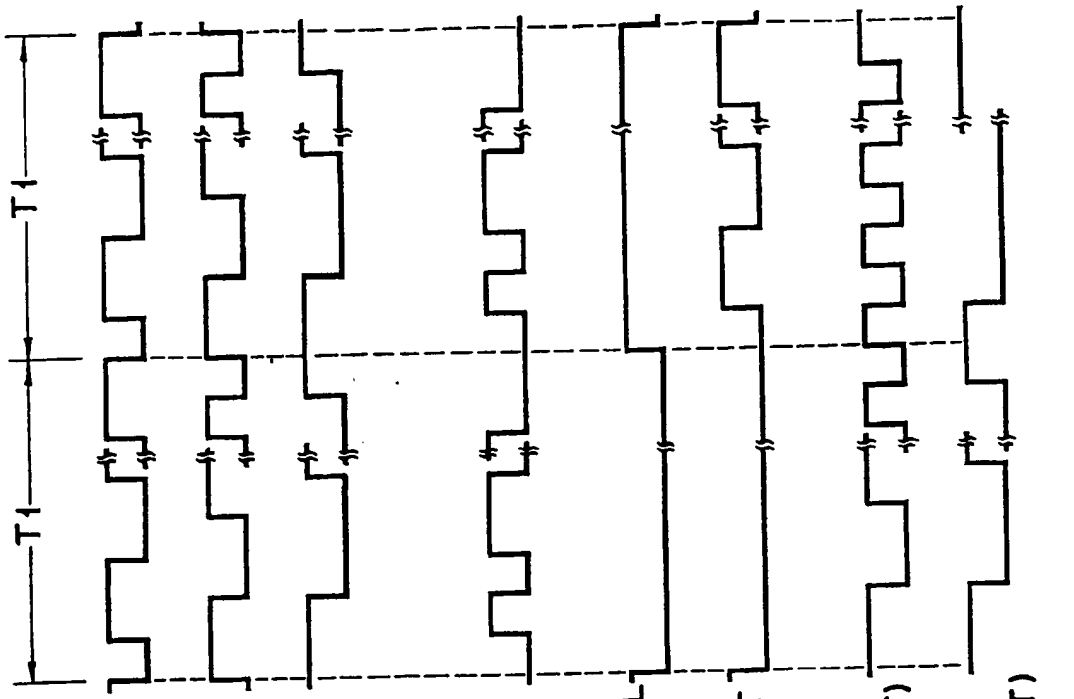

FIG. 5A

FIG. 5B

FIG. 5C

FIG. 5D

FIG. 5E

FIG. 5F

FIG. 5G

FIG. 5H

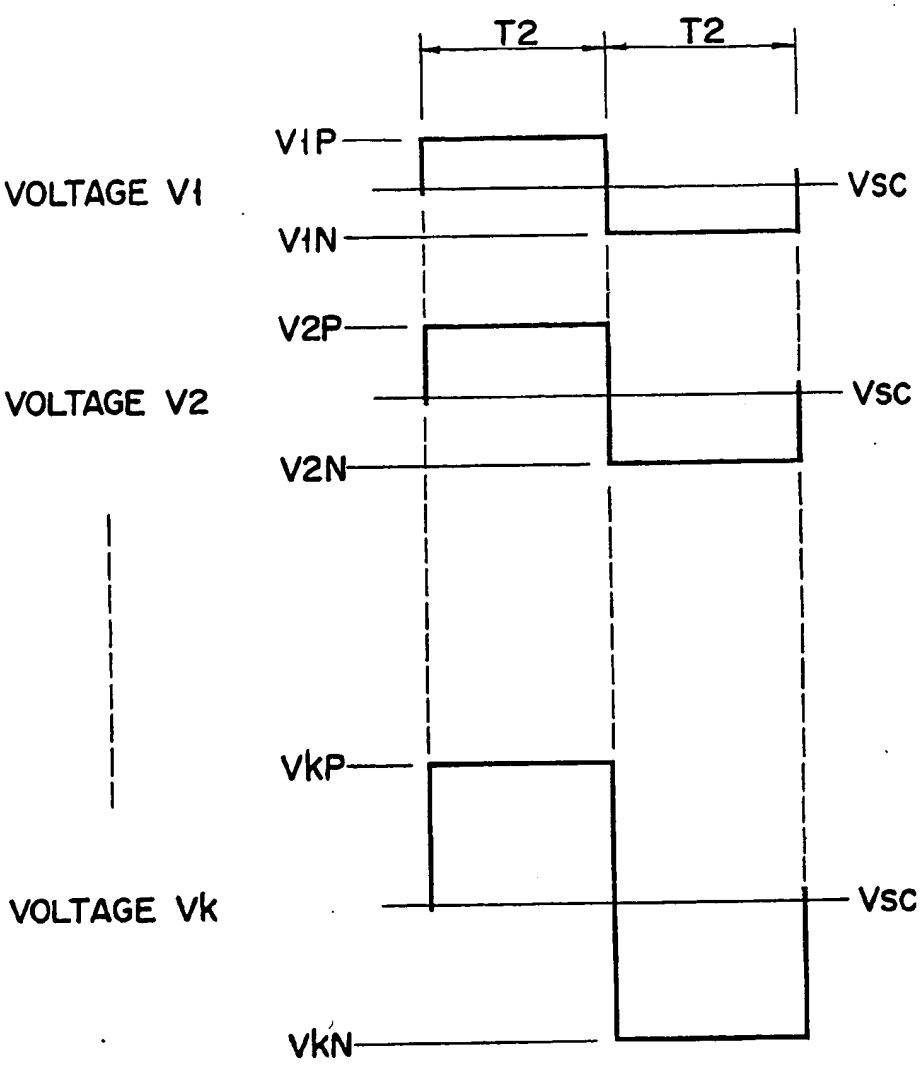
T2
T2
V1P
VOLTAGE V1
VSC
V1N
V2P
VOLTAGE V2
VSC
V2N
VkP
VOLTAGE Vk
VSC
VkN

FIG. 6

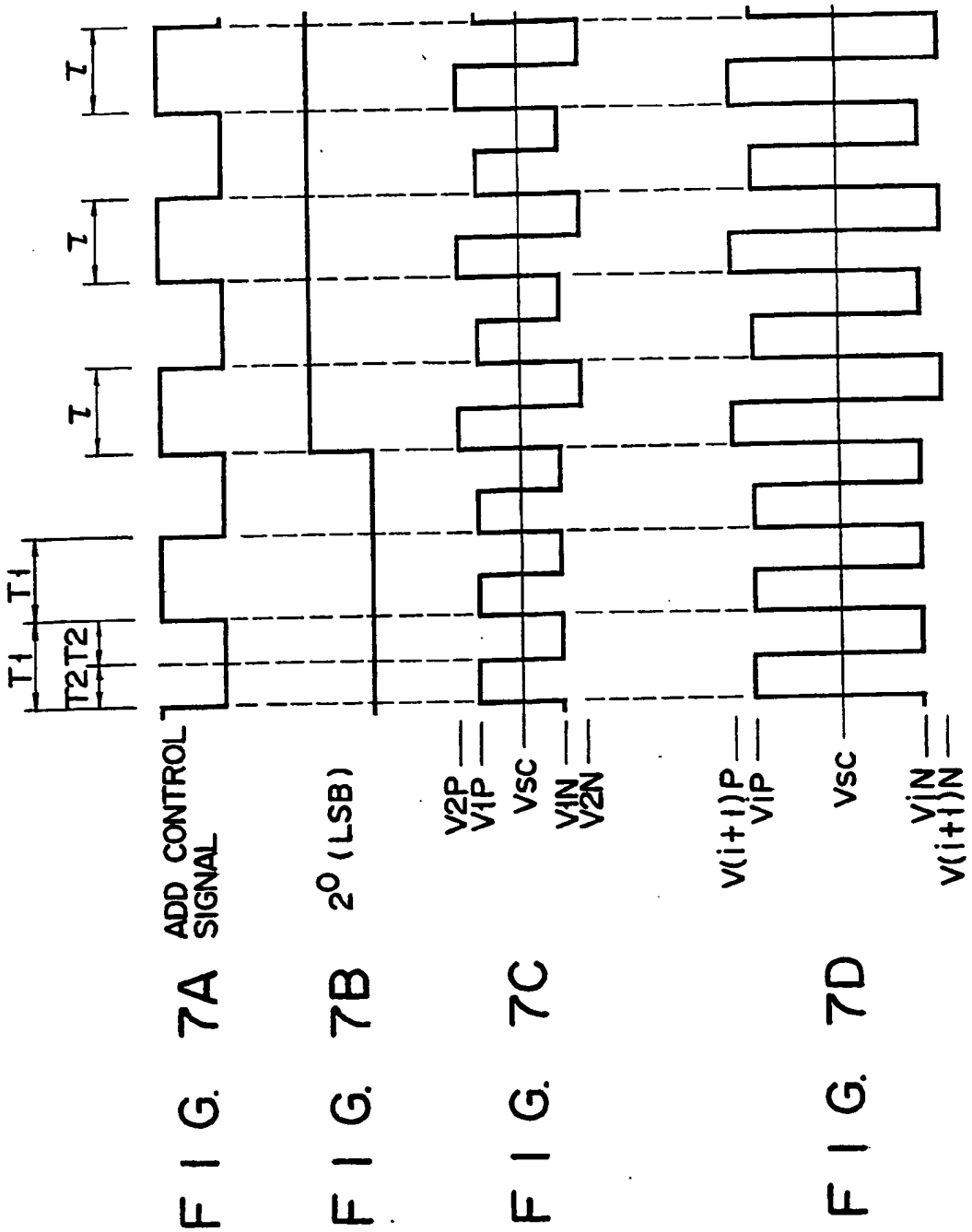

FIG. 7A

FIG. 7B

FIG. 7C

FIG. 7D

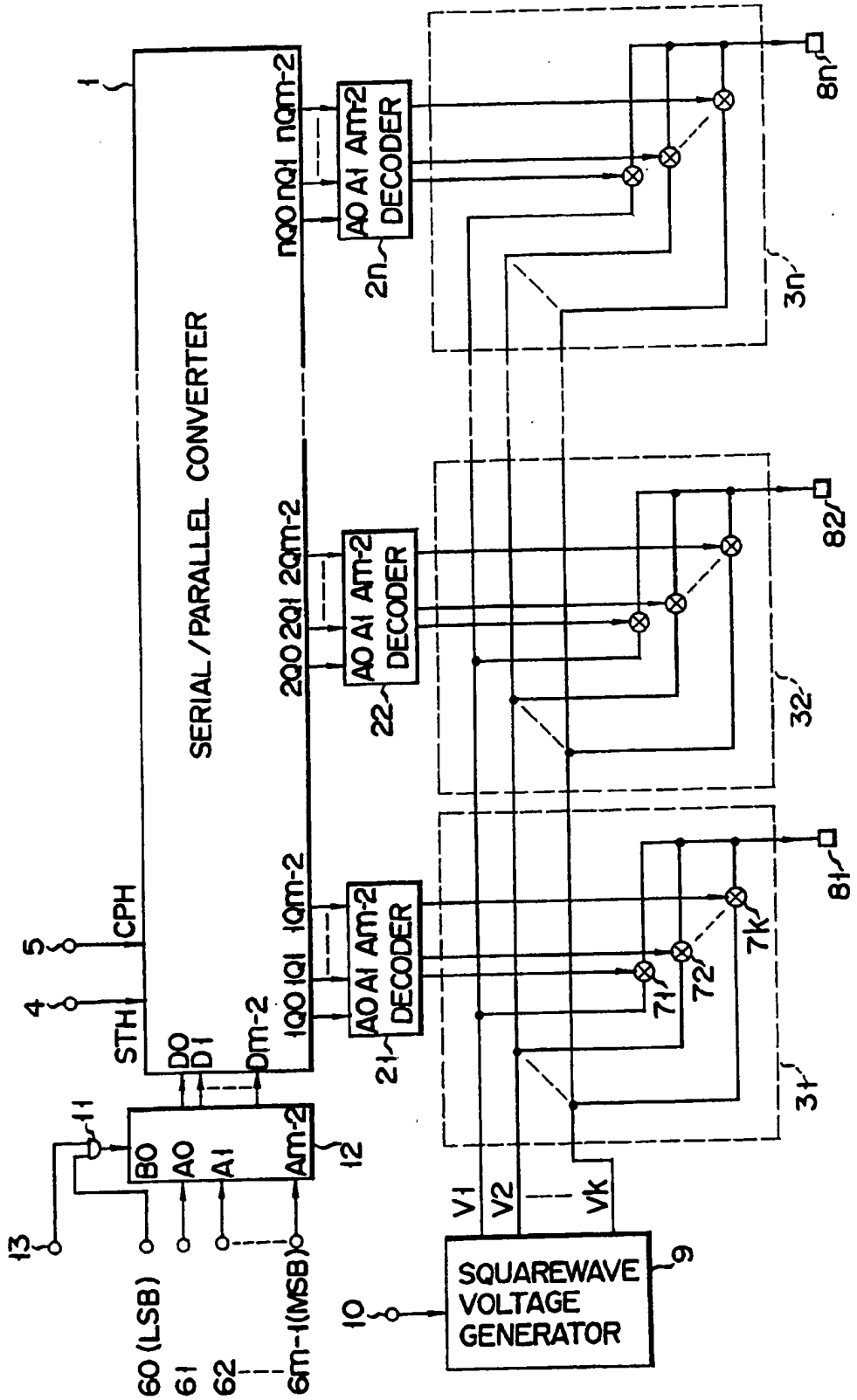
SERIAL/PARALLEL CONVERTER
DECODER
SQUAREWAVE VOLTAGE GENERATOR
CPH
STH
DO
D1
Dm-2
BO
AO
A1
Am-2
V1
V2
Vk
60 (LSB)
61
62
6m-1(MSB)

FIG. 8

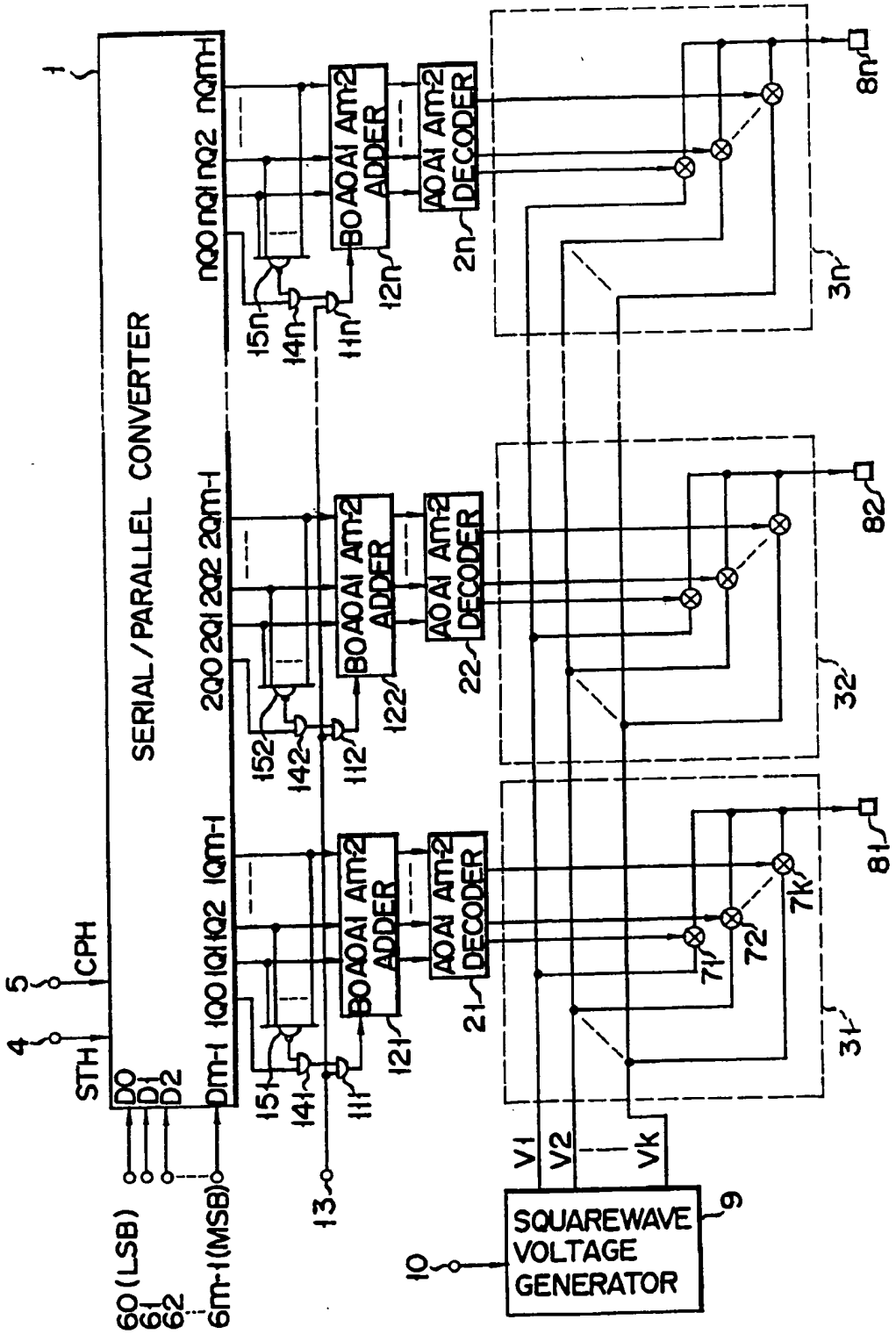
SERIAL/PARALLEL CONVERTER
STH
CPH
SQUAREWAVE VOLTAGE GENERATOR
ADDER
DECODER

FIG. 9

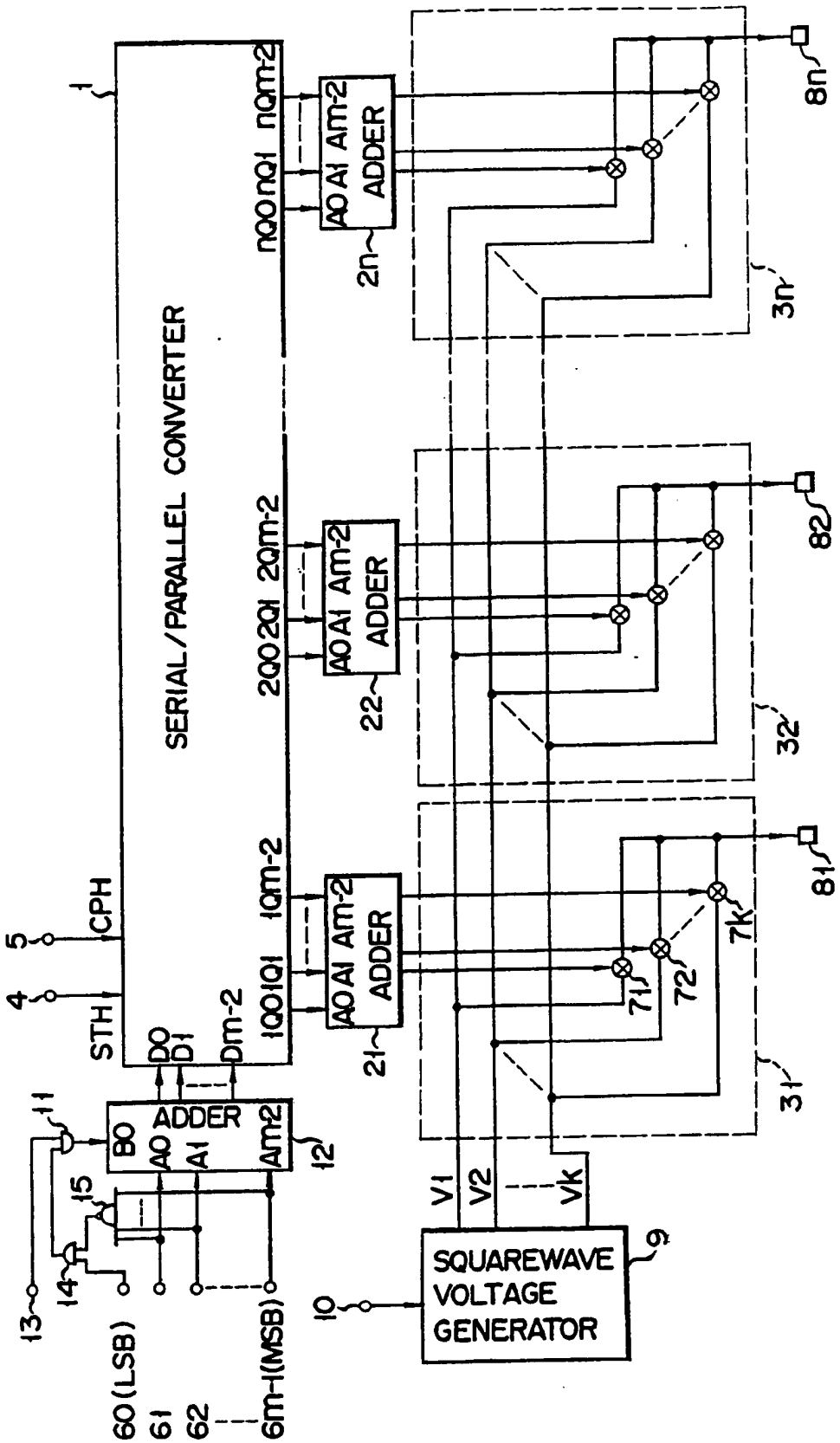
SERIAL/PARALLEL CONVERTER
CPH
STH
DO
D1
Dm-2
ADDER
BO
AO
A1
Am-2
SQUAREWAVE VOLTAGE GENERATOR
V1
V2
Vk
60(LSB)
61
62
6m-1(MSB)
nQ0 nQ1 nQm-2
2Q0 2Q1 2Qm-2
1Q0 1Q1 1Qm-2
2n
22
21
3n
32
31
8n
82
81
71
72
7k

FIG. 10

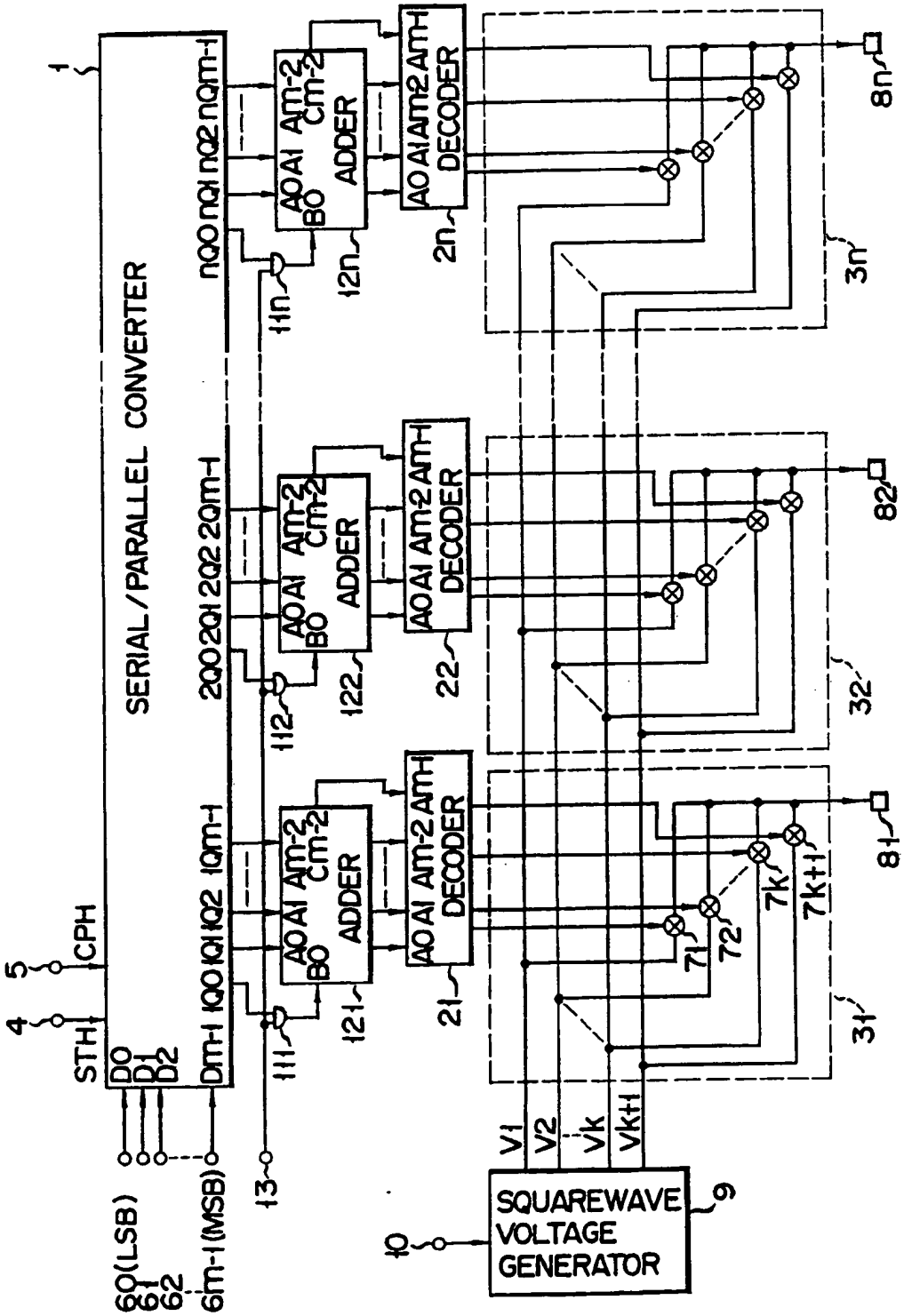
SERIAL/PARALLEL CONVERTER
ADDER
DECODER
SQUAREWAVE VOLTAGE GENERATOR
CPH
STH
D0
D1
D2
60(LSB)
61
62
6m-1(MSB)
13
10
9
V1
V2
Vk
Vk+1
81
82
8n
31
32
3n
71
72
7k
7k+1
21
22
2n
111
112
11n
121
122
12n

FIG. 11

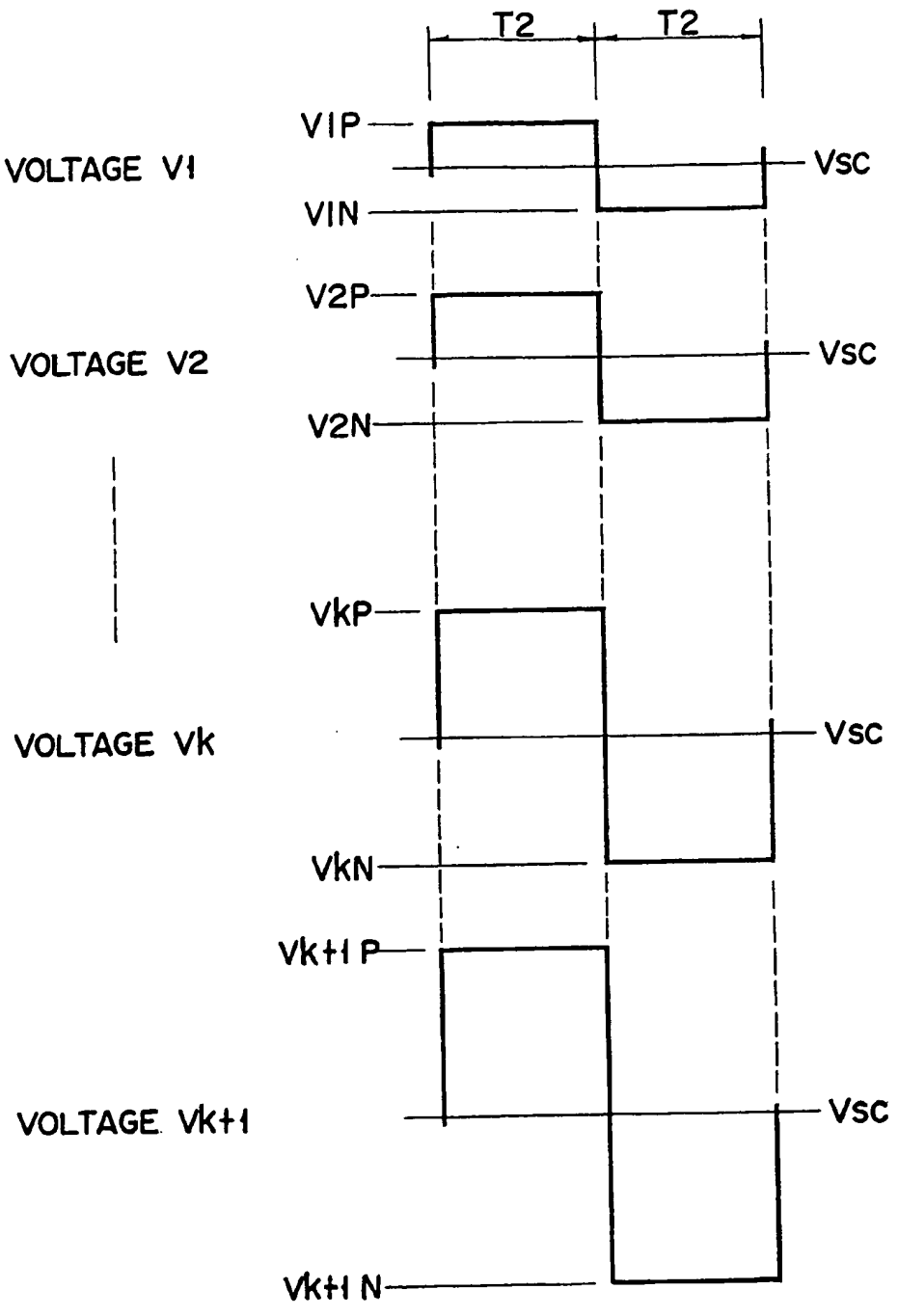
T2
T2
VOLTAGE V1
V1P
VIN
Vsc
VOLTAGE V2
V2P
V2N
Vsc
VOLTAGE Vk
VkP
VkN
Vsc
VOLTAGE Vk+1
Vk+1 P
Vk+1 N
Vsc

FIG. 12

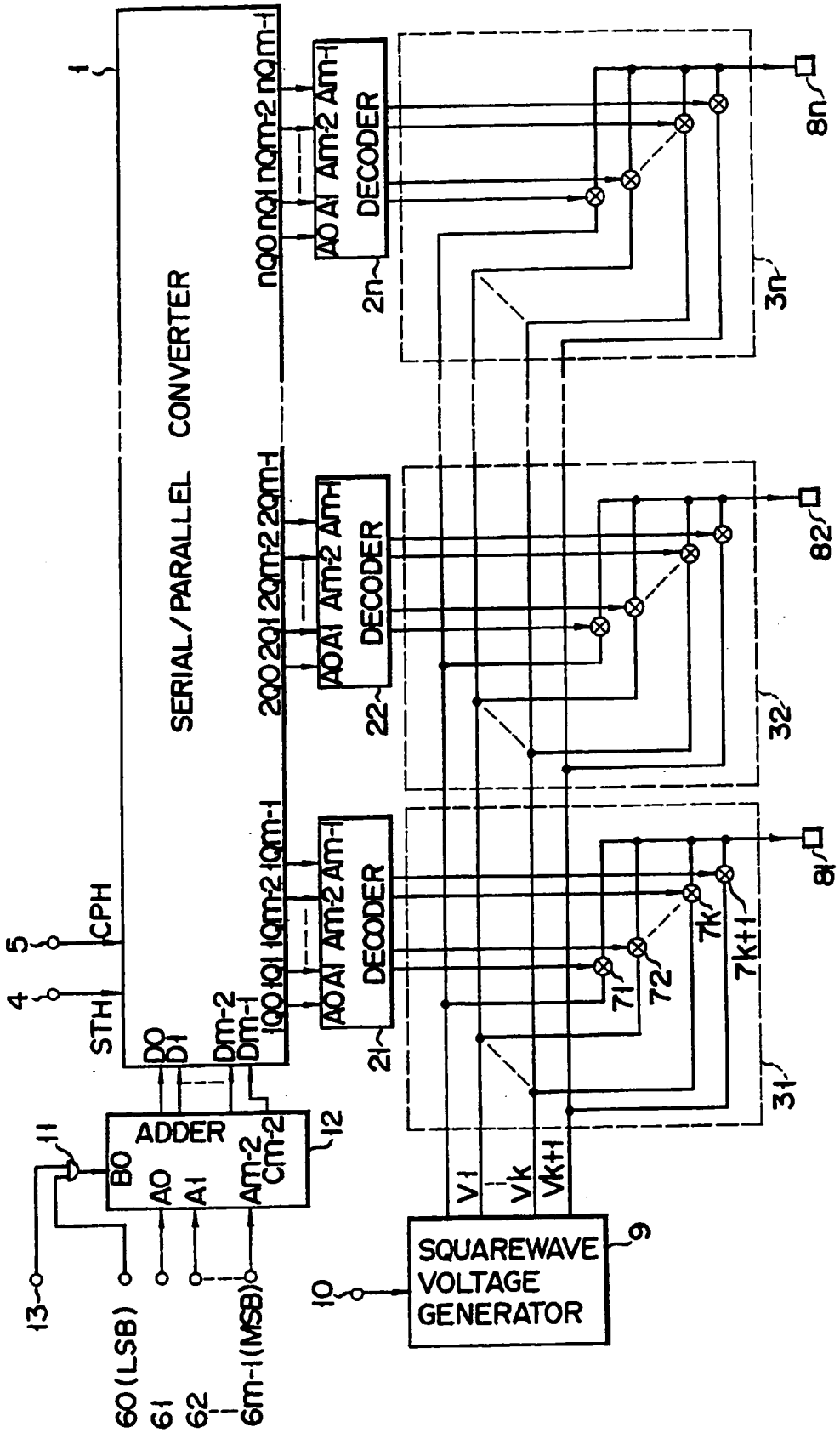
SERIAL/PARALLEL CONVERTER
DECODER
DECODER
DECODER
ADDER
SQUAREWAVE VOLTAGE GENERATOR
CPH
STH
8n
82
81
3n
32
31
2n
22
21
9
10
11
12
13
60(LSB)
61
62
6m-1(MSB)
V1
Vk
Vk+1
71
72
7k
7k+1

FIG. 13